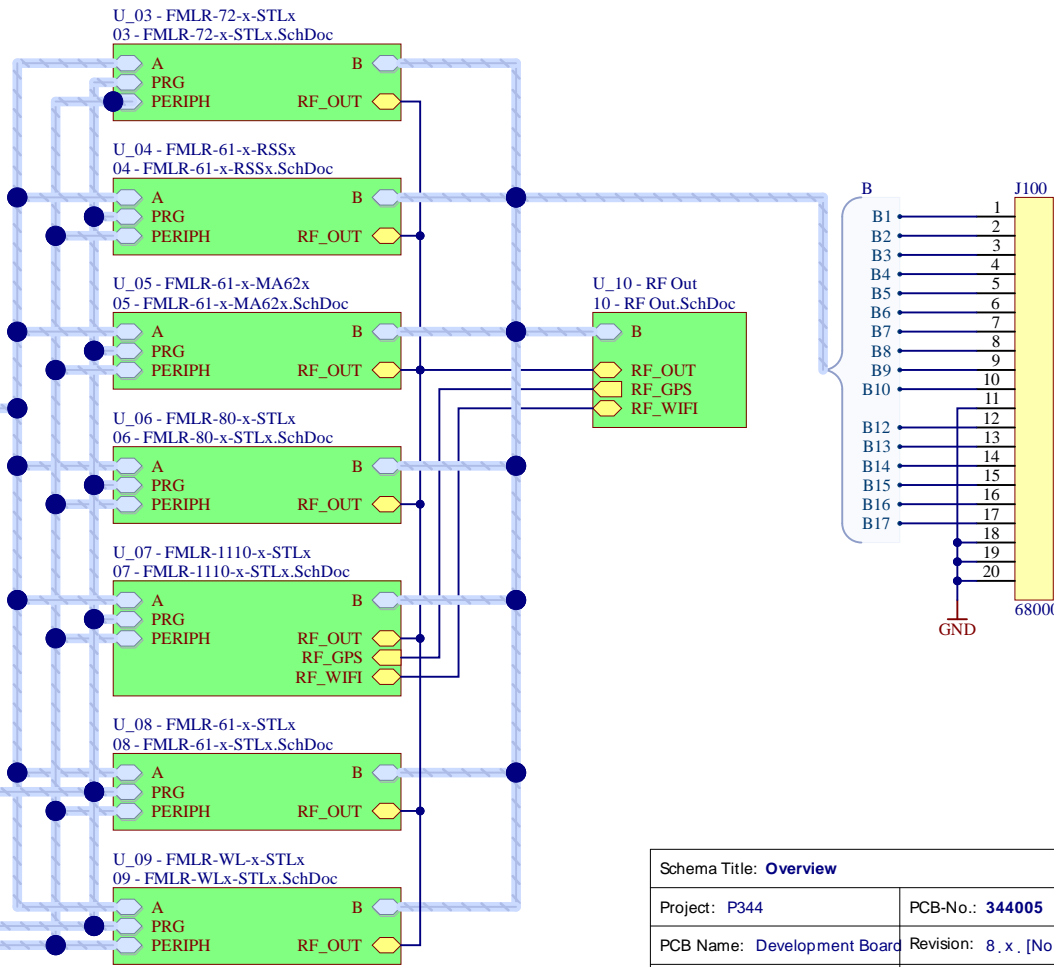
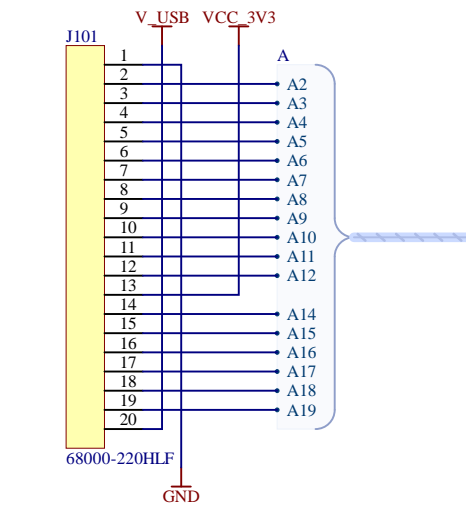


Revision	Date	Description	Signed
1.0	17.06.2019	initial project creation	DS
2.0	1.10.2019	replaced senslab chip with FTDI	DS
2.1	25.11.2019	changed project name, changed renesas jumper variant	SU
3.0	19.12.2019	solder jumper replaced with tht jumper	DS
4.0	30.11.2020	added Maxim Module to Dev Board	DS
5.0	11.01.2021	added RF matching for MAXIM Module	DS
6.0	27.07.2021	change maxim module dc/dc converter add SX1280 module	SU
7.G	13.04.2022	Add Segger on-board debugger	LP
8.H	13.10.2022	Add Segger logo and WLE variant	LP

Variant	Name	Description	Date	Signed
1	DEV-FMLR-STEVK1	EVK FMLR STM SX1272 modules, FMLR-72-U-STL0Z-4M	17.06.2019	DS
2	DEV-FMLR-RSEVK2	EVK FMLR Renesas SX1261 modules, FMLR-61-U-RSS3-4M	17.06.2019	DS
3	DEV-FMLR-MAEVK3	EVK FMLR Maxim SX1261 modules, FMLR-61-P-MA625	20.11.2020	DS
4	DEV-FMLR-STEVK4	EVK FMLR STM SX1280 modules, FMLR-80-U-STL4E-4M	27.07.2021	SU
5	DEV-FMLR-STEVK5	EVK FMLR STM SX1261, FMLR-61-U-STL0Z-4M	13.10.2021	LP
6	DEV-FMLR-STEVK6	EVK FMLR STM LR1110, FMLR-1110-U-STL0Z-4M	27.07.2021	SU
7	DEV-FMLR-STEVK7	EVK FMLR STM32WLE5, FMLR-WL-U-STE5-4M	13.10.2021	LP

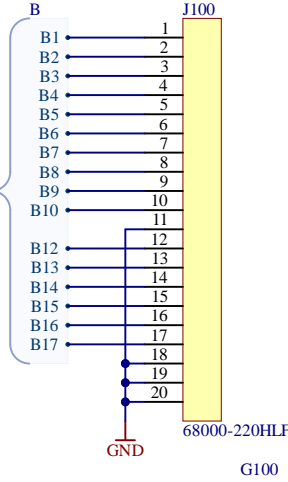


Variant used for output data: [No Variat

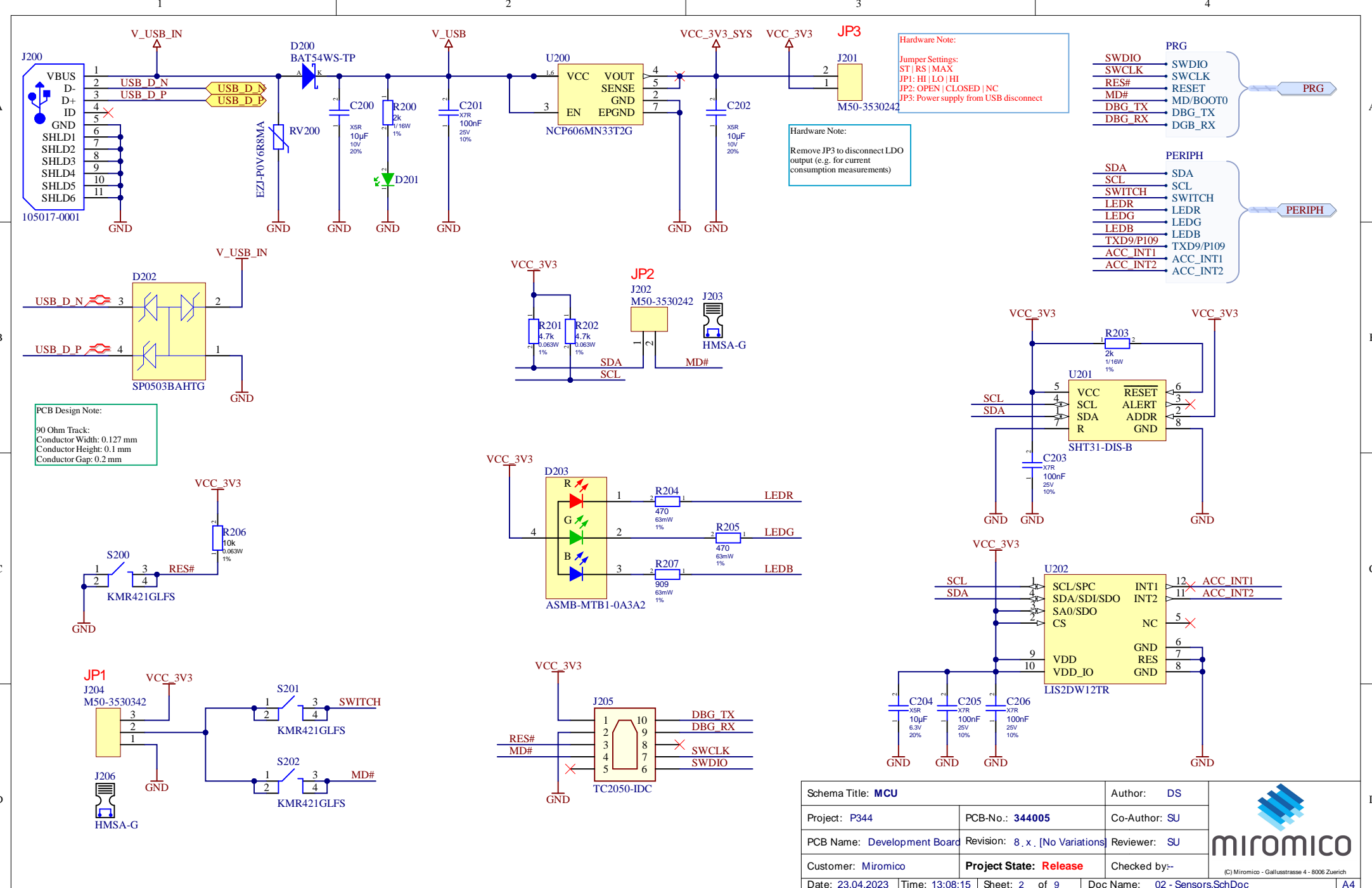
Hardware Note:  
Notes regarding the Hardware - e.g. Function


Software Note:  
Notes regarding the Software - e.g. Function, Address

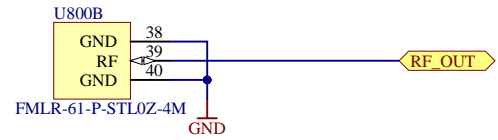
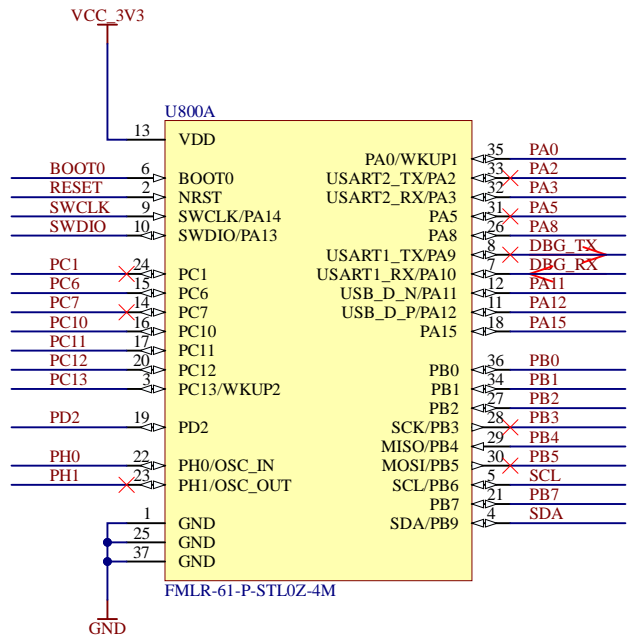
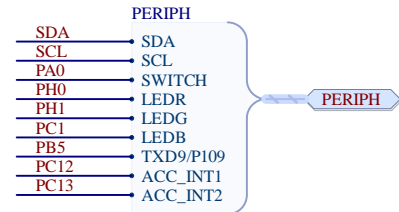
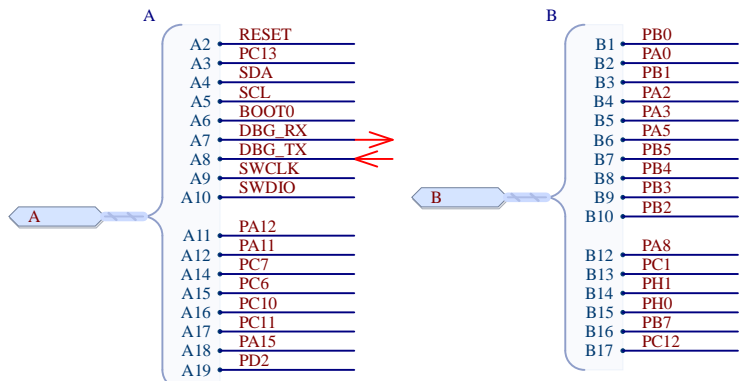
PCB Design Note:  
Notes regarding the PCB Design - e.g. specific Design requirement




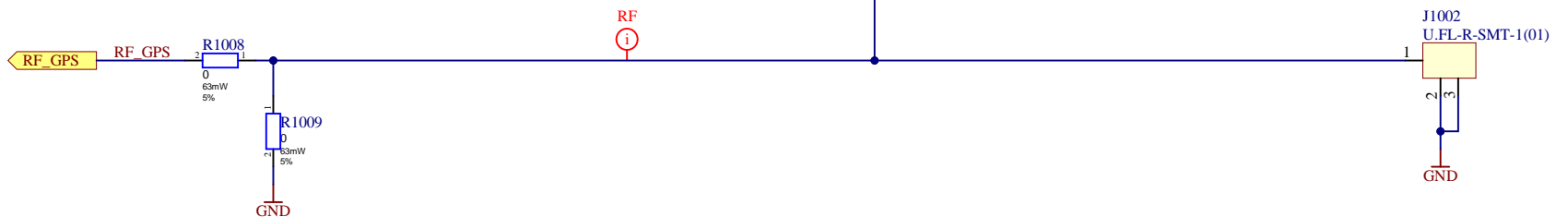
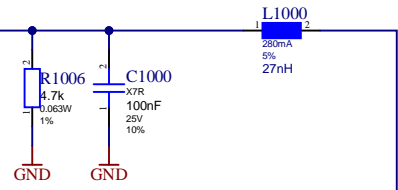
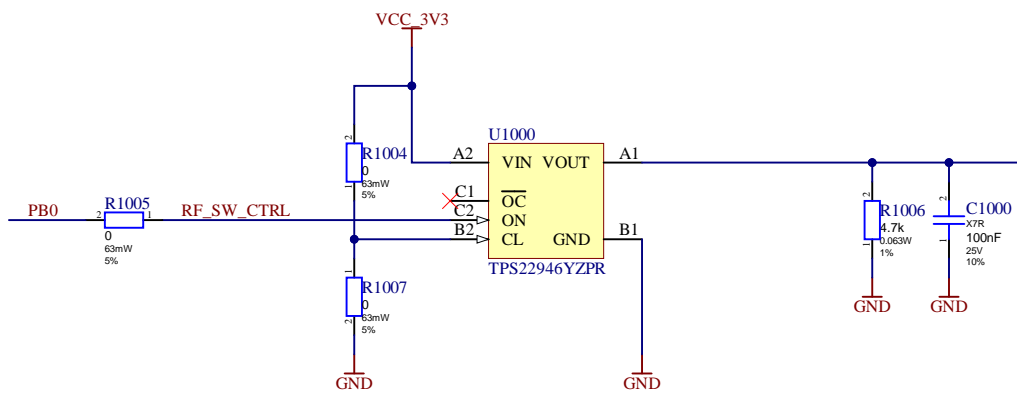
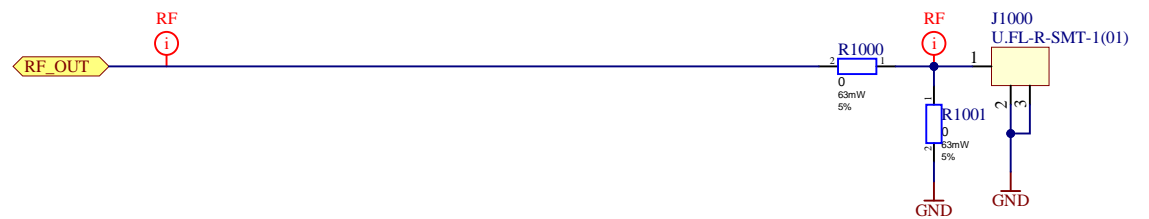
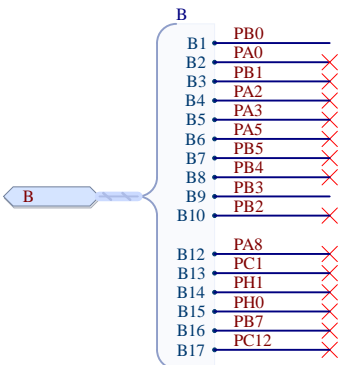
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Project: P344	PCB-No.: 344005	Co-Author: SU	
PCB Name: Development Board	Revision: 8_x_ [No Variations]	Reviewer: SU	
Customer: Miromico	Project State: <b>Release</b>	Checked by:-	
Date: 23.04.2023	Time: 13:08:15	Sheet: 1 of 9	Doc Name: 01 - Overview.SchDoc




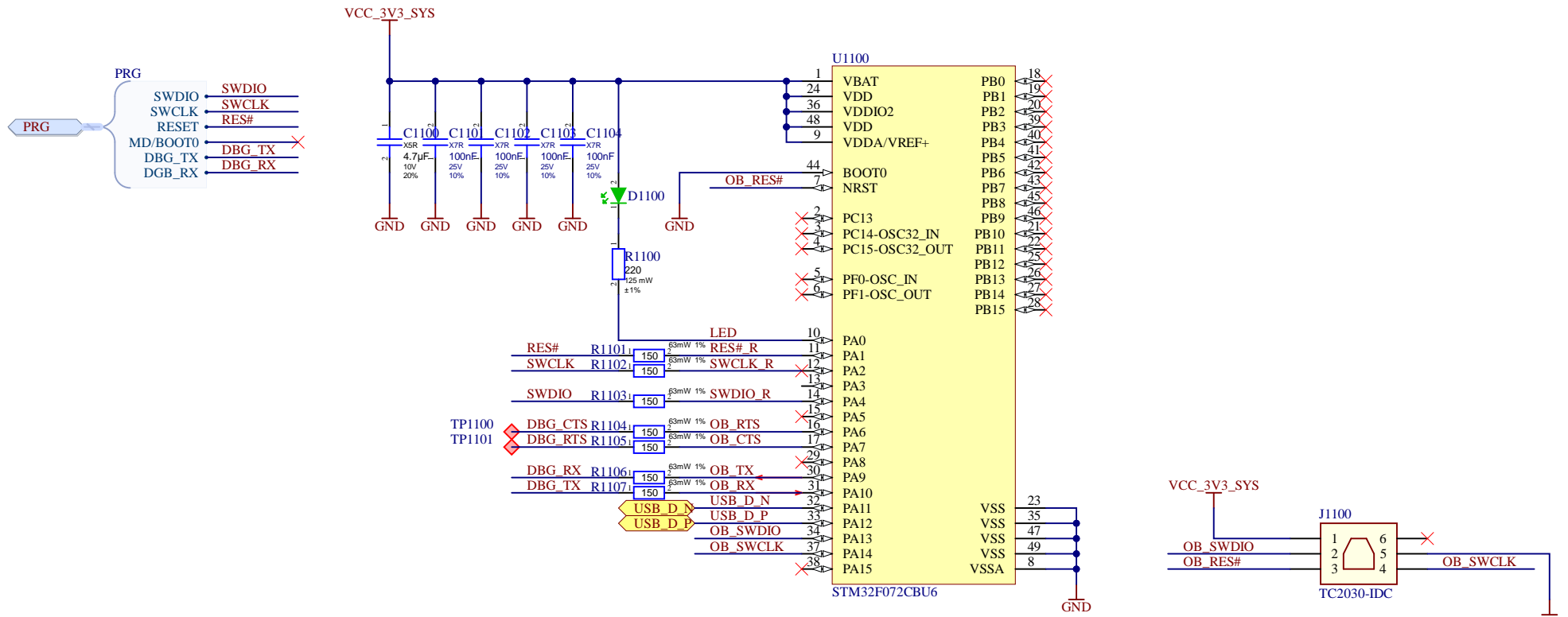
Schema Title: <b>MCU</b>		Author: DS	 (C) Miromico - Gallusstrasse 4 - 8006 Zuerich
Project: P344	PCB-No.: <b>344005</b>	Co-Author: SU	
PCB Name: Development Board	Revision: 8 . x . [No Variations]	Reviewer: SU	
Customer: <b>Miromico</b>	<b>Project State: Release</b>	Checked by:-	
Date: 23.04.2023	Time: 13:08:15	Sheet: 2 of 9	Doc Name: 02 - Sensors.SchDoc




Schema Title: <b>MCU</b>		Author: <b>DS</b>	 (C) Miromico - Gallusstrasse 4 - 8006 Zuerich
Project: <b>P344</b>	PCB-No.: <b>344005</b>	Co-Author: <b>SU</b>	
PCB Name: <b>Development Board</b>	Revision: <b>8_x_x [No Variations]</b>	Reviewer: <b>SU</b>	
Customer: <b>Miromico</b>	<b>Project State: Release</b>	Checked by:-	
Date: <b>23.04.2023</b>	Time: <b>13:08:16</b>	Sheet: <b>8</b> of <b>*</b>	
Doc Name: <b>08 - FMLR-61-x-STLx.SchDoc</b>		<b>A4</b>	



Schema Title: <b>MCU</b>		Author: <b>DS</b>	 (C) Miromico - Gallusstrasse 4 - 8006 Zuerich
Project: <b>P344</b>	PCB-No.: <b>344005</b>	Co-Author: <b>SU</b>	
PCB Name: <b>Development Board</b>	Revision: <b>8_x_x [No Variations]</b>	Reviewer: <b>SU</b>	
Customer: <b>Miromico</b>	<b>Project State: Release</b>	Checked by:-	
Date: <b>23.04.2023</b>	Time: <b>13:08:17</b>	Sheet: <b>10 of 9</b>	
Doc Name: <b>10 - RF Out.SchDoc</b>		<b>A4</b>	



PCB Design Note:  
Factory programming port - place on bottom side of PCB

Schema Title: <b>On-Chip Debugger</b>		Author: <b>DS</b>	 (C) Miomico - Gallusstrasse 4 - 8006 Zuerich
Project: <b>P344</b>	PCB-No.: <b>344005</b>	Co-Author: <b>SU</b>	
PCB Name: <b>Development Board</b>	Revision: <b>8.x.x [No Variations]</b>	Reviewer: <b>SU</b>	
Customer: <b>Miomico</b>	<b>Project State: Release</b>	Checked by:-	
Date: <b>23.04.2023</b>	Time: <b>13:08:17</b>	Sheet: <b>11</b> of <b>9</b>	
Doc Name: <b>11 - Debugger.SchDoc</b>			